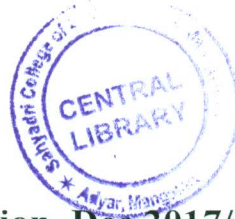


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10CS33

Third Semester B.E. Degree Examination, Dec.2017/Jan.2018

Logic Design

Time: 3 hrs.

Max. Marks:100

Note: Answer any FIVE full questions, selecting at least TWO questions from each part.

PART – A

- 1 a. What is a digital electronic circuit? List the applications of digital circuits and systems. (04 Marks)
- b. With an aid of a circuit diagram, explain the operation of a 2-input standard TTL NAND gate with totem-pole output. Show that NAND gate is an universal logic gate. (08 Marks)
- c. Explain sourcing and sinking current, noise immunity, standard loading and output-input profile of standard TTL device. (08 Marks)
- 2 a. Realize a logic circuit using only NAND gates that converts a 4-bit binary input to a Gray-code output. Use Karnaugh maps for simplification of logic expressions. (12 Marks)
- b. Find the simplified expression of, $Y = f(A, B, C, D) = \sum m(0, 3, 4, 5, 6, 7, 11, 14)$ using Quine-Mccluskey method. (08 Marks)
- 3 a. Design a full adder circuit using a 3-to-8 decoder and multi-input OR gates. Write VHDL / verilog code for a 2 to 4 decoder. (06 Marks)
- b. Explain how a 7446 decoder-driver is used to drive a common anode seven-segment indicator. (06 Marks)
- c. Distinguish :
 - (i) PAL and PROM.
 - (ii) PLA and PAL.
 - (iii) Encoder and multiplexer.
 - (iv) Even parity and odd parity. (08 Marks)
- 4 a. What is a Schmitt trigger? Show how it can be used to ensure rapid switching action. (04 Marks)
- b. Show how to use a simple RS latch to eliminate switch contact bounce. (06 Marks)
- c. Show how SR flip-flop is converted into JK flip-flop and explain how racing problem in JK flip-flop is avoided. Write VHDL/verilog code for JK flip-flop. (10 Marks)

PART – B

- 5 a. What is a shift register? How long will it take to shift an 8-bit number into a 74164 shift register if the clock is set at 10 MHz? (04 Marks)
- b. Explain the working of 4-bit parallel-access shift register 7495. Show how it can be wired for shift left operation. (08 Marks)
- c. Discuss the advantages and disadvantages of a ring counter. Also write VHDL/verilog code for a twisted tail counter. (08 Marks)
- 6 a. Realize a 3-bit asynchronous binary up-down counter using J-K flip-flops and basic logic gates. (06 Marks)
- b. Design a modulo-4 synchronous counter using J-K flip flops. (10 Marks)
- c. Realize a sequence generator circuit using synchronous counter to generate a repetitive sequence of binary word 1011 with minimum number of memory elements. (04 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.



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- 7 a. Distinguish Moore model and Mealy model of sequential logic system. (04 Marks)
b. What is an ASM chart? Draw the ASM chart of a sequence generator that receives binary data stream at its input, X and signals when a combination '011' arrives at the input by making its output, Y high which otherwise remains low. Consider Moore model. (08 Marks)
c. Discuss the problems with asynchronous sequential logic circuits. (08 Marks)
- 8 a. What is a binary ladder DAC? Mention its advantages over the resistance divider DAC. Also explain accuracy and resolution of DAC. (06 Marks)
b. Explain the working of a 2-bit flash A/D converter. List its applications. (08 Marks)
c. Explain the successive approximation technique of A/D conversion. When is it useful? (06 Marks)

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